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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,827	01/03/2001	Ashok Krishnamurthi	0023-0027	9945
44987	7590	03/07/2006	EXAMINER	
HARRITY SNYDER, LLP 11350 Random Hills Road SUITE 600 FAIRFAX, VA 22030				LEE, ANDREW CHUNG CHEUNG
			ART UNIT	PAPER NUMBER
			2664	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/752,827	KRISHNAMURTHI ET AL.
	Examiner	Art Unit
	Andrew C. Lee	2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 24 October 2005.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-10, 12-15, 17-21 and 23-27 is/are rejected.

7) Claim(s) 11, 16 and 22 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 4, 2, 20, 25, 5, 6, 7, 13, 9, 15, 10, 23, 12, 17, 18, 19, 24, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy et al. (US 6636515 B1) in view of Skirmont et al. (US 6385209 B1).

Regarding claims 1, 4, Roy et al disclose the limitation of an apparatus for interfacing a high-speed link to a network device (Abstract, lines 1 – 7; column 2, lines 39 – 41), comprising a receiver module (Fig. 1A, element 12; column 9, lines 59 – 67, “the receive side SONET interface”), operating at a first clock rate, for receiving a stream of in-coming data from the high-speed link (column 9, lines 59 – 67, first clock rate is cited as “ a one-bit 622 MHZ clock”; column 10, lines 1 – 4); a framer module (Fig. 1A, element 14), operating at a second clock rate, for deserializing the stream of in-coming data onto a multi-line bus and extracting data packets from the deserialized data on the multi-line bus (Fig. 2, column 9, lines 59 – 67; column 10, lines 4 – 16, second clock

rate is cited as “ a one-bit 155 MHZ clock”), wherein the second clock rate is lower than the first clock rate (column 10, lines 1 – 4, 155MHz clock is slower than first clock rate is cited as “ a one-bit 622 MHZ clock). Roy et al do not disclose expressly a sprayer module to receive the extracted data packets from the framer module and, for each of the extracted packets, select one of a plurality of processing paths in the network device and transmit the extracted packet to the selected processing path (). Skirmont et al. disclose the limitation of a sprayer module to receive the extracted data packets from the framer module and, for each of the extracted packets, select one of a plurality of processing paths in the network device and transmit the extracted packet to the selected processing path (Fig. 6, column 1, 66 – 67, column 2, lines 1 – 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roy et al. to include a sprayer module to receive the extracted data packets from the framer module and, for each of the extracted packets, select one of a plurality of processing paths in the network device and transmit the extracted packet to the selected processing path such as that taught by Skirmont et al. in order to provide method and apparatus for implementing a single higher-capacity port from a plurality of lower-capacity ports (as suggested by Skirmont et al. see, column 1, lines 9 – 11).

Regarding claims 2, 20, 25, Roy et al disclose the limitation of an apparatus for interfacing a high-speed link to a network device (Abstract, lines 1 – 7; column 2, lines 39 – 41), Roy et al. do not disclose expressly the receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-192 link. Skirmont et al. disclose the limitation of the receiver module comprising optics and circuitry for receiving optical

signals from a SONET OC-192 link (Fig. 4, 5, 6, "OC-192c", column 4, lines 50 – 50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roy et al. to include a receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-192 link such as that taught by Skirmont et al. in order to to provide method and apparatus for implementing a single higher-capacity port from a plurality of lower-capacity ports (as suggested by Skirmont et al. see, column 1, lines 9 – 11).

Regarding claim 5, Roy et al disclose the apparatus wherein the plurality of processing paths includes a plurality of switching/forwarding module for switching or forwarding the extracted data packets (Fig. 2, column 6, lines 18 – 25, recited switch element including twelve "datapath and link bandwidth arbitration modules"; lines 37 – 45).

Regarding claim 6, Roy et al. disclose the apparatus wherein the sprayer module is configured to transmit each extracted data packet to one of the plurality of preprocessing modules (column 12, lines 7 – 28; 48 – 50). However, Roy et al. do not disclose expressly the apparatus wherein the sprayer module is configured to transmit each extracted data packet to one of the plurality of preprocessing modules based on a load balancing technique. Skirmont et al. disclose the limitation of transmitting each extracted data packet to one of the plurality of preprocessing modules based on a load balancing technique (column 5, lines 57 – 65; Load balancing). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roy et al. to include an apparatus wherein the sprayer module is configured to transmit

each extracted data packet to one of the plurality of preprocessing modules based on a load balancing technique such as that taught by Skirmont et al. in order to provide methods and apparatus for implementing a single higher-capacity port from a plurality of lower-capacity ports (as suggested by Skirmont et al., see column 1, lines 9 – 11).

Regarding claims 7,13, Roy et al disclose the limitation of the apparatus comprising a plurality of memories, each memory corresponding to one of the plurality of preprocessing modules (column 12, lines 31 – 37) and each preprocessing module comprises a memory management module for storing portions of data packets into its corresponding memory (column 12, lines 34 – 41, data descriptor).

Regarding claims 9, 15, Roy et al. disclose the apparatus comprising the receiver module, the framer module, the sprayer module, the plurality of preprocessing modules, the plurality of memories integrated onto a single chip (see column 25 – 470, Appendix A, iTAP Service Processor Chip Specification and column 471 –556, Appendix B, ITAP Switch Chip Engineering Specification “Chiron Chip”).

Regarding claims 10, 23, Roy et al disclose the limitation of the apparatus comprising a deframer module (Fig. 1A, element 40; column 15, lines 16 – 21), operating at the second clock rate, for receiving data packets and processing the data packets into a stream of outgoing data for transmission on the high-speed link (Fig 1A, element 40, column 16, lines 12 – 26); a transmitter module, operating at the first clock rate, for transmitting the stream of out-going data onto the high-speed link (Fig. 1A, column 16, lines 23 – 26).

Regarding claim 12, Roy et al disclose the limitation of an apparatus for interfacing at least one line interface card to a plurality of switching/forwarding modules of a network device (Fig. 2; column 24, lines 8 – 13), comprising a plurality of preprocessing modules for processing data packets and transmitting the processed data packets to respective switching/forwarding modules (Fig. 2, column 6, lines 18 – 28 recited switch element including twelve “datapath and link bandwidth arbitration modules”; lines 37 – 45; lines 37 – 45; column 24, lines 8 – 13); Roy et al do not disclose expressly a sprayer module for receiving data packets from at least one line interface card and, for each received data packet, selecting one of the plurality of preprocessing modules and transmitting the received data packet to the selected preprocessing module. Skirmont et al. disclose the limitation of a sprayer module for receiving data packets from at least one line interface card and, for each received data packet, selecting one of the plurality of preprocessing modules and transmitting the received data packet to the selected preprocessing module (Fig. 6, column 1, 66 – 67, column 2, lines 1 – 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roy et al. to include a sprayer module for receiving data packets from at least one line interface card and, for each received data packet, selecting one of the plurality of preprocessing modules and transmitting the received data packet to the selected preprocessing module such as that taught by Skirmont et al. in order to provide method and apparatus for implementing a single higher-capacity port from a plurality of lower-capacity ports (as suggested by Skirmont et al. see, column 1, lines 9 – 11).

Regarding claim 17, Roy et al disclose the limitation of a networking device comprising a sprayer module for receiving data packets and, for each of the data packets, selecting one of a plurality of channels and outputting the data packet on the selected channels (Fig. 1A, elements 16, 18, 20, 22; column 10, lines 65 – 67; column 11, lines 1 – 6; columns 27 – 28; Receive Direction for the Figure 1, iTAP Port Processor Overview, Columns 29 – 30, the description); a plurality of preprocessing modules for processing data packets, each preprocessing module receiving data packets from one of the channels of the sprayer module (Fig. 1A, elements 16, 18, 20, 22, column 12, lines 1 – 9); and a plurality of switching/forwarding modules, each switching/forwarding module receiving data packets from a corresponding one of the plurality of preprocessing modules (Fig. 2, column 6, lines 18 – 28; lines 37 – 45; column 24, lines 8 – 13).

Regarding claim 18, Roy et al disclose a framer module operating at a first clock rate, for deserializing the stream of in-coming data onto a multi-line bus and extracting data packets from the deserialized data on the multi-line bus and transmitting the extracted data packets to the sprayer module (Fig. 2, column 10, lines 4 – 6; 8 – 16).

Regarding claim 19, Roy et al disclose the limitation of a network device comprising a receiver module, operating at a second clock rate, for receiving a stream of in-coming data from a high-speed link and transmitting of in-coming data to the framer module (Fig. 2, column 10, lines 2 – 4); wherein the first clock rate is lower than the second clock rate (column 10, lines 2 – 6).

Regarding claim 24, Roy et al disclose the limitation of the networking device comprising a transmitter module, operating at a second clock rate for transmitting the stream of out-going data onto the high-speed link (Fig. 1A, column 16, lines 23 – 26, lines 37 – 38), wherein the first clock rate is lower than the second clock rate (column 10, lines 2 – 6).

Regarding claim 27, Roy et al disclose the limitation of receiving data from a high-speed link (*Fig 1A*), comprising deserializing the stream of data signals onto a multi-line bus (Fig. 1A, element 12, column 9, lines 60 – 62); extracting data packets from the serialized data (Fig. 1A, element 12, column 9, lines 60 – 67); Roy et al. does not disclose expressly spraying the data packets across a plurality of processing paths according to a load balancing or hashing technique; receiving a stream of data signals at a data rate of at least approximately 10 Gigabits per second. Skirmont et al. disclose the limitation of spraying the data packets across a plurality of processing paths according to a load balancing or hashing technique (column 5, lines 57 – 65; Load balancing); receiving a stream of data signals at a data rate of at least approximately 10 Gigabits per second (column 1, lines 63 – 65, “10 Gigabit Ethernet “). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roy et al. to include spraying the data packets across a plurality of processing paths according to a load balancing or hashing technique; receiving a stream of data signals at a data rate of at least approximately 10 Gigabits per second such as that taught by Skirmont et al. in order to provide method and apparatus for implementing a

single higher-capacity port from a plurality of lower-capacity ports (as suggested by Skirmont et al. see, column 1, lines 9 – 11).

4. Claims 3, 21, 26, 8, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy et al (US 6646983 B1) and Skirmont et al. (US 6385209 B1) as applied to claims 1, 4, 2, 20, 25, 5, 6, 7, 13, 9, 15, 10, 23, 12, 17, 18, 19, 24, 27 above, and further in view of in view of Ben-Zur et al. (US 6754174 B1).

Regarding claims 3, 21, 26, Roy et al disclose the limitation of an apparatus for interfacing a high-speed link to a network device (Abstract, lines 1 – 7), Roy et al do not disclose expressly the receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-768 link. Ben-Zur et al. disclose the limitation of the receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-768 link (Fig. 2, column 5, lines 1 – 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roy et al to include a receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-768 link such as that taught by Ben-Zur et al. in order to have an increasing the efficiency of SONET communications by minimizing the response time for the performance of protection switching (as suggested by Ben-Zur et al., see column 1, lines 10 – 12).

Regarding claims 8, 14, Roy et al disclose the limitation of an apparatus for interfacing a high-speed link to a network device (Abstract, lines 1 – 7; column 2, lines 39 – 41), Roy et al disclose the apparatus comprising the receiver module, the framer

module, the sprayer module, the plurality of preprocessing modules, the plurality of memories (Fig 1A, Fig 1B and Fig 2). Roy et al do not disclose expressly the apparatus mounted onto a single board. Ben-Zur et al. disclose the limitation of the apparatus mounted onto a single board (column 5, lines 18 – 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Roy et al to include the apparatus comprising the receiver module, the framer module, the sprayer module, the plurality of preprocessing modules, the plurality of memories are mounted onto a single board such as that taught by Ben-Zur et al. in order to have an increasing the efficiency of SONET communications by minimizing the response time for the performance of protection switching (as suggested by Ben-Zur et al., see column 1, lines 10 – 12).

Allowable Subject Matter

5. Claims 11, 16, 22 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

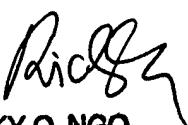
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ACL

Feb 13, 2006



RICKY Q. NGO
PATENT EXAMINER